AMENDMENTS TO THE SPECIFICATION

Please amend the first full paragraph at unnumbered page 10, beginning at line 17, of the English translation of the Specification as follows:

In order to resolve this problem, the present invention proposes the arrangement of a register 30, as illustrated in Figure 2, in parallel to the memory element 2, which, in the presence of a release signal "enable" stores a sampled value $S_{in}(k)$ of the input signal, and ~~which is~~ that has its output side connected to the ~~output~~ input side of the interpolation element 3, in the exemplary embodiment, to the half-band filter 4. Moreover, "range 2" from Figure 8 is supplemented by the polyphase p_{10}.

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LAW OFFICES OF
CHRISTENSEN O'CONNOR JOHNSON KINDNESS PLLC
1420 Fifth Avenue
Suite 2800
Seattle, Washington 98101
206.682.8100